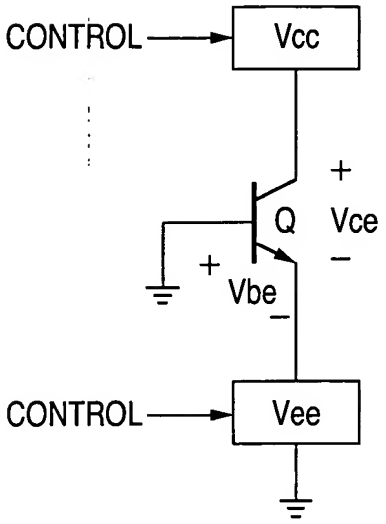

FIG. 1A
(PRIOR ART)

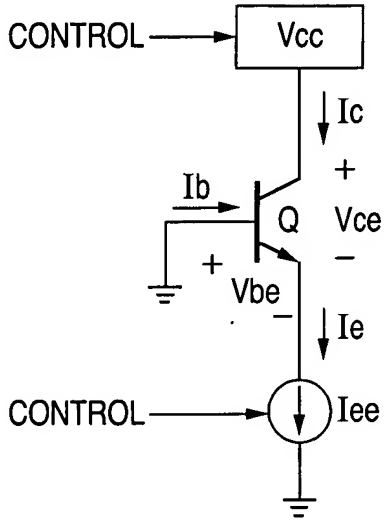

FIG. 2A
(PRIOR ART)

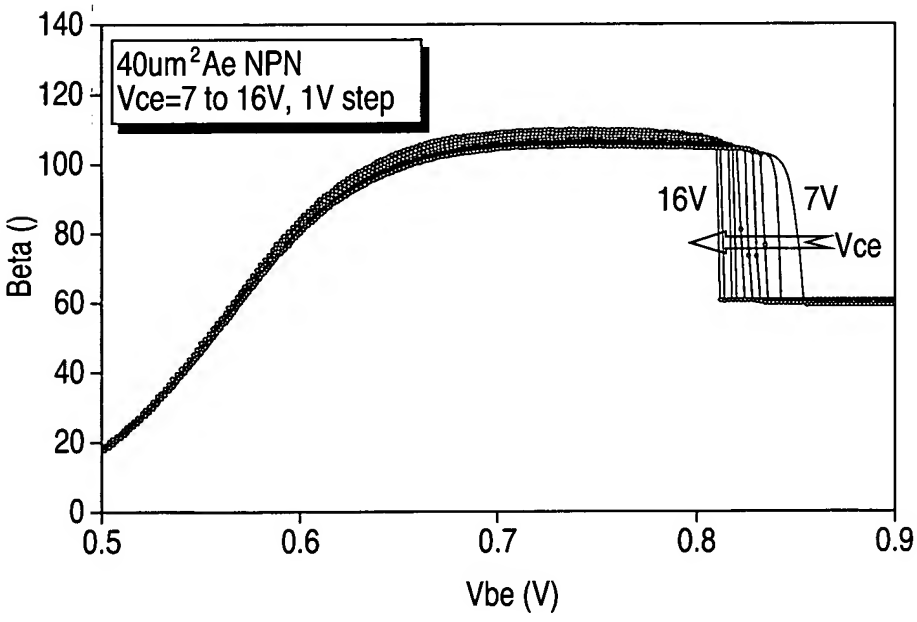

FIG. 1B
(PRIOR ART)

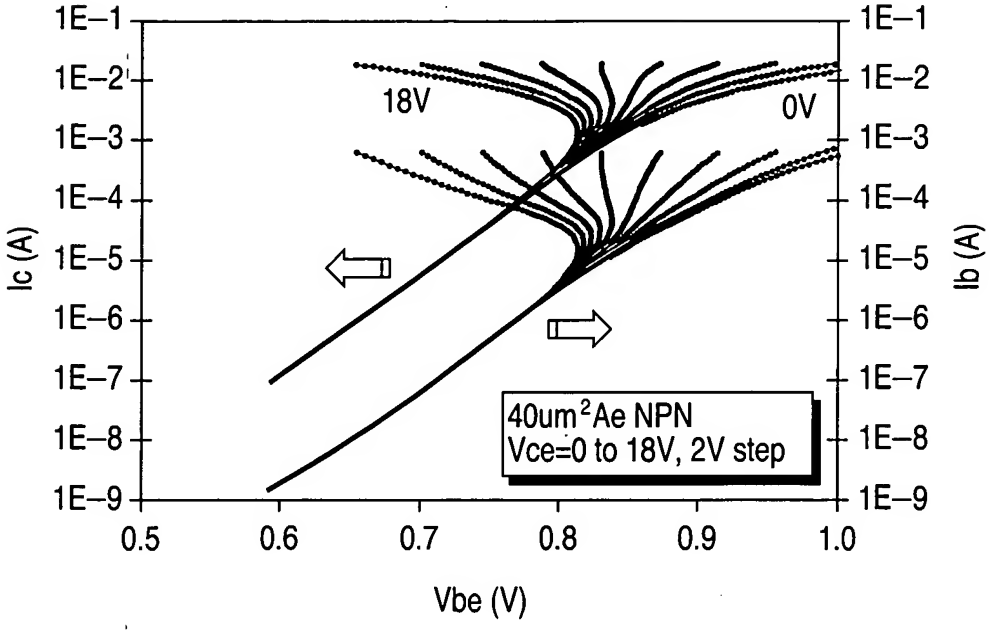

FIG. 2B
(PRIOR ART)

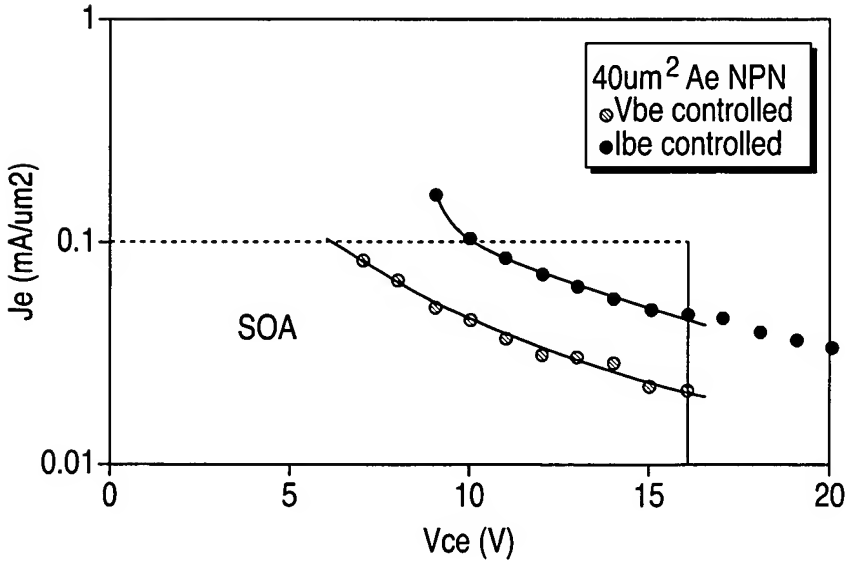

FIG. 3
(PRIOR ART)

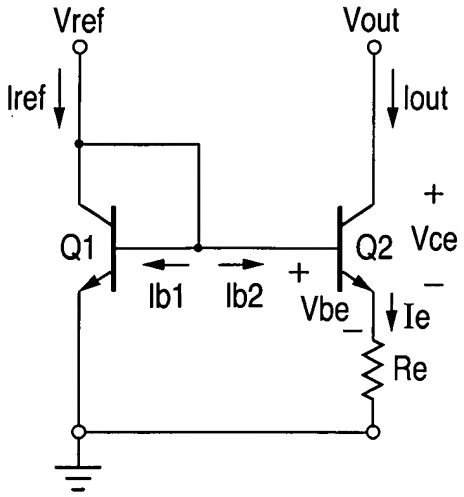

FIG. 4

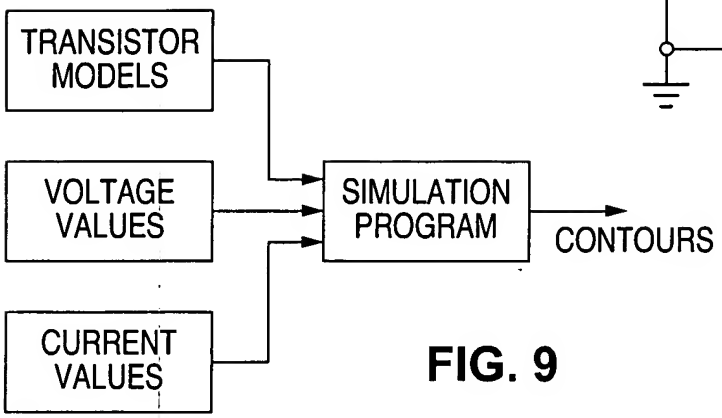

FIG. 9

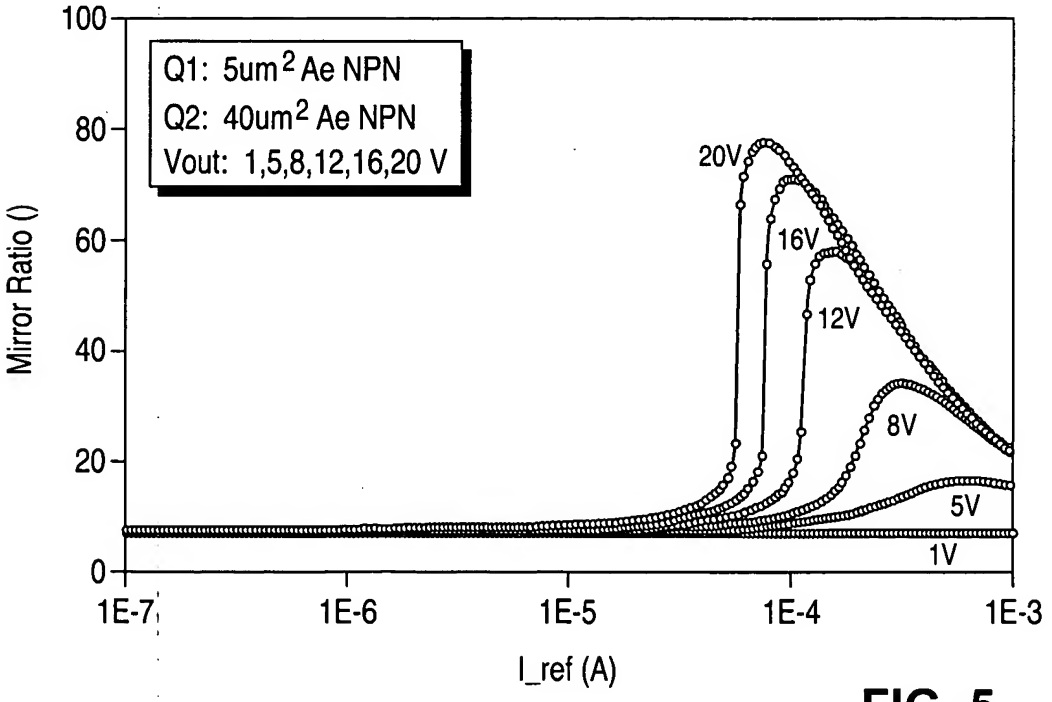

FIG. 5

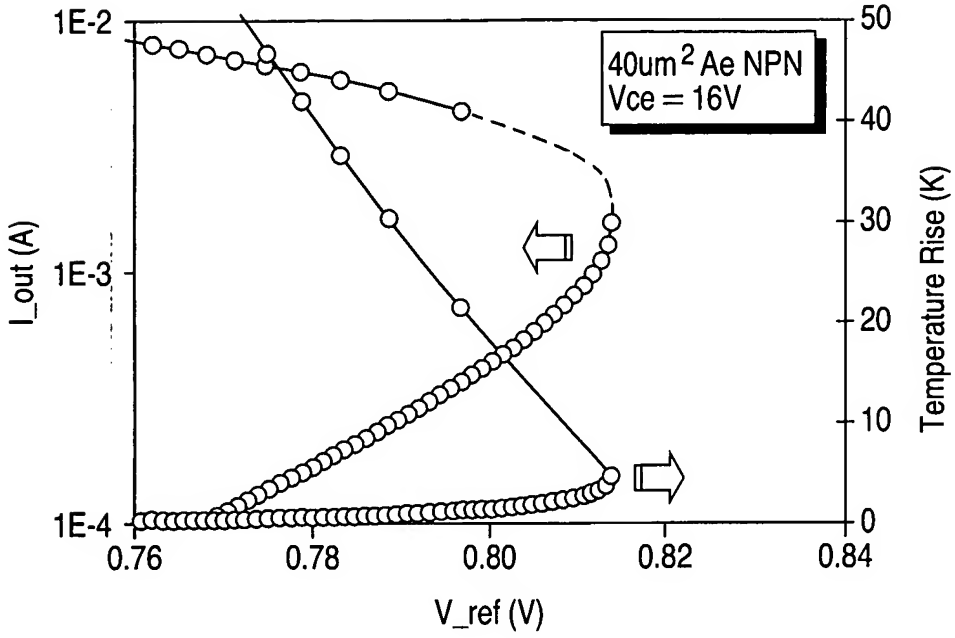
1E-2
1E-3
1E-4
I_out (A)
40um2 Ae NPN
Vce = 16V
50
40
30
20
10
0
Temperature Rise (K)
0.76
0.78
0.80
0.82
0.84
V_ref (V)

FIG. 6

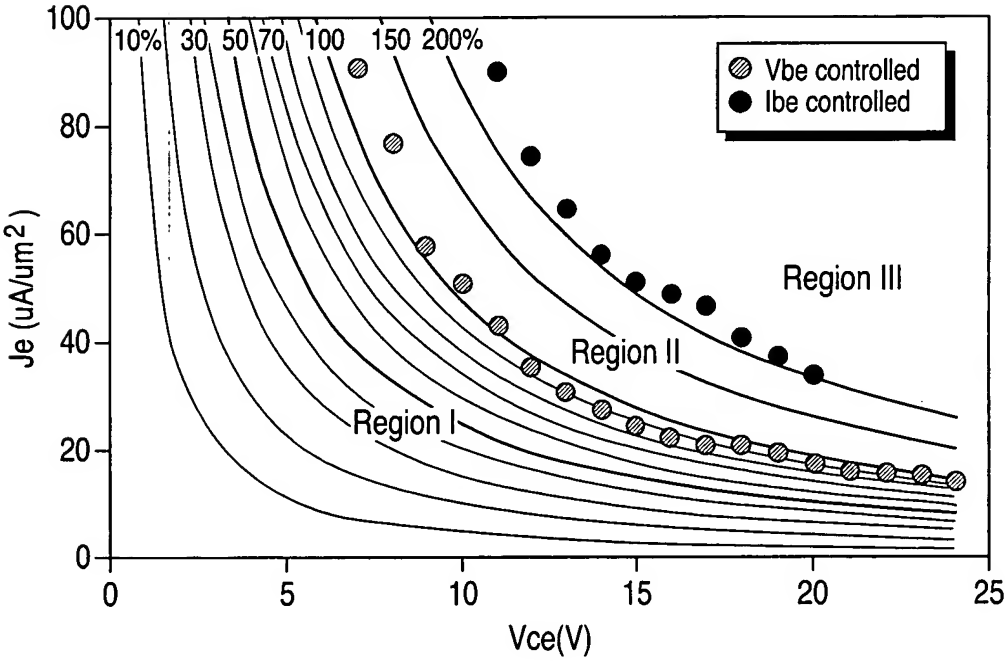
100
80
60
40
20
0
Je (uA/um2)
10%
30
50
70
100
150
200%
Vbe controlled
Ibe controlled
Region I
Region II
Region III
0
5
10
15
20
25
Vce(V)

FIG. 8

METHOD FOR QUANTIFYING SAFE OPERATING AREA
FOR BIPOLAR JUNCTION TRANSISTOR
Inventor: Kim et al.
Application No.: 10/688,550

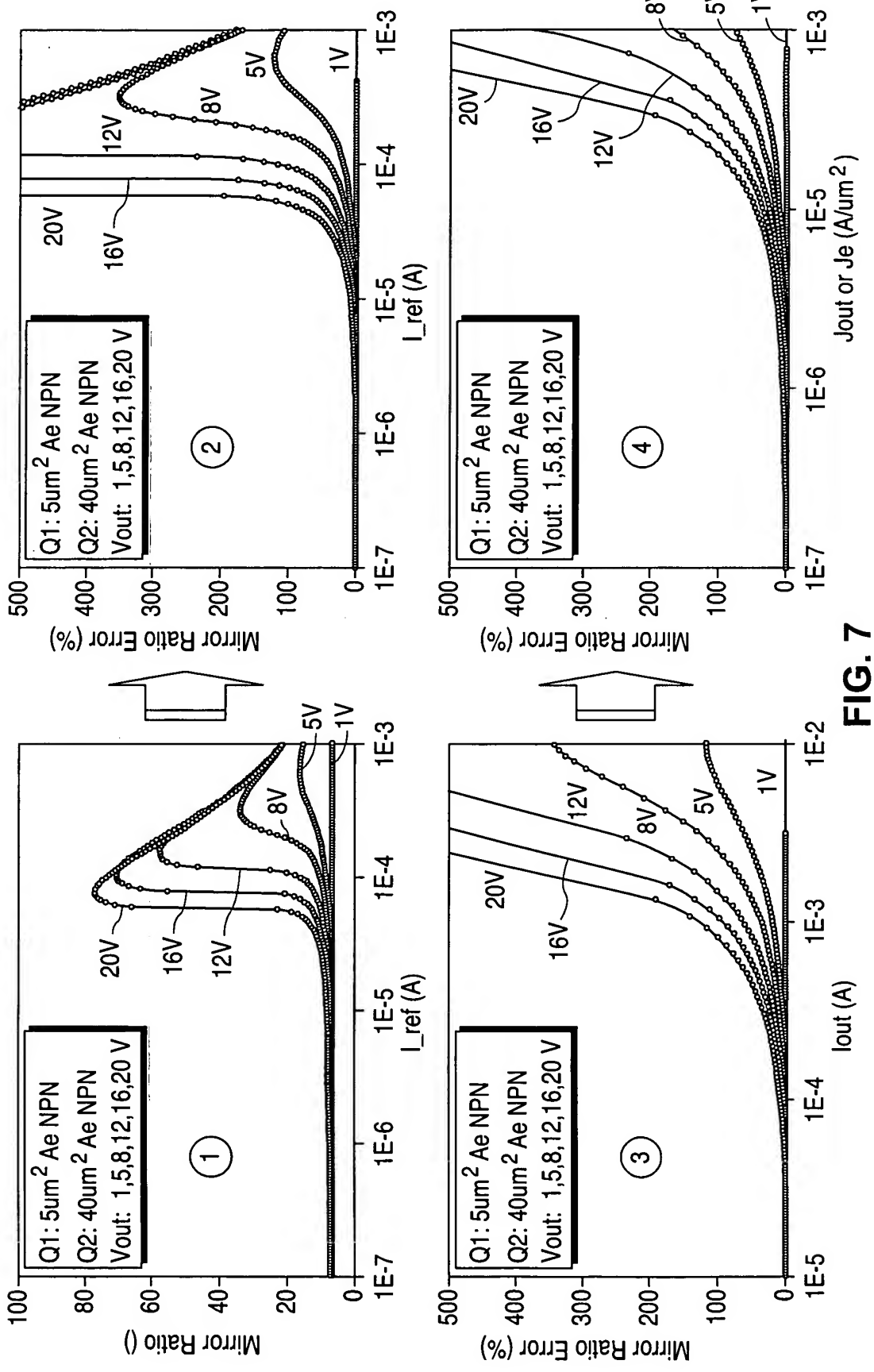

FIG. 7